Q_1: Fill in blanks

1- In a counter with N flip-flops having a modulus of less than or equal to 2^N, the maximum usable clock frequency is given by ----.

2- The maximum count of the counter is ----.

3- The Boolean expression of D_A for (3,0,6) synchronous is ----.

4- D flip- flop is used as a frequency division since the time of the next flip-flop in counter equal to ---- the time of the first one.

5- The difference state in binary for a counter divided by 5000 using 74HC161 four bits counter only is ----.

Q_2: design a register that transfers the data (10110101001) to the left using four (D) flip-flops, and draw the outputs of these flip-flops after seven pulses.

Q_3: Design (*3bits*) mod 3 up and down an asynchronous counter .